ABSTRACT:

An electronic device (100) has a data storage device (120) for storing N data elements, the data storage device (120) comprising a first collection (122) of data storage elements (130). The first collection (122) of data storage elements (130) is accessible through an address decoder (140). In a shift register mode of the data storage device (120), the address decoder (140) is responsive to an address generator (160) comprising a modulo-N counter. Rather than having to shift data elements from one data storage element (130) to another, the address generator (160) generates a pointer to the data storage element (130) that contains the data element that is to be shifted out of the shift register. This has the advantage that the output of a predecessor data storage element (130) in a shift register need not be interconnected to the input of its successor. In addition, the amount of data traffic required during a shift is drastically reduced. The invention is particularly relevant to reconfigurable logic devices that use look-up tables for implementing shift registers.

Fig.1